The Analysis of the Power Loss in a Zero-Voltage Switching Two-Inductor Boost Cell Operating under Different Circuit Parameters

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Abstract-**This paper studies a comprehensive set of power loss components in a current fed Zero-Voltage Switching (ZVS) two-inductor boost cell and presents a power loss optimisation method. The ZVS two-inductor boost cell is fed from a sinusoidally modulated two-phase synchronous buck converter with an interphase transformer (IPT). The ZVS boost cell produces a rectified sinusoidal voltage, which can be applied to an unfolding stage to generate grid compatible voltage as part of a module integrated photovoltaic inverter. This paper conducts the numerical analysis of the average power loss and establishes a set of circuit parameters for an optimized operating point, which results in the minimal power loss in the ZVS boost cell. The experimental results for a 1 MHz 100 W ZVS two-inductor boost converter are presented.**

I. INTRODUCTION

The two-inductor boost converter offers significant advantages in the applications such as photovoltaic (PV) systems, where low dc input voltages need to be transformed to high dc output voltages, [1]. Most recently, Module Integrated Converters (MICs) have been proposed as an attractive alternative in the grid interactive PV applications, [2]. In such applications, a high power density is certainly one of the most desirable features, which calls for high switching frequency operations. However, a high switching loss, together with the transformer leakage inductance, becomes an inherent barrier for the hard-switched converter to obtain an acceptable efficiency under high switching frequency operations. In order to remove the switching loss and actively utilize the transformer leakage inductance, a Zero-Voltage Switching (ZVS) two-inductor boost converter has been developed as a dc-dc conversion stage in the MICs, [3]. Fig. 1 shows the ZVS converter with an inverter. In the soft-switched two-inductor boost converter, the parasitic components including the transformer leakage inductance and the mosfet output capacitance are absorbed into the resonant network. This enables the mosfet to turn on at zero voltage, resulting in a theoretical zero switching loss. In this voltage fed converter, the switch duty ratio is fixed and the dc link offers a fixed voltage to the following dc-ac inverter. In order to generate low frequency grid compatible voltage waveforms, the Pulse-Width Modulation (PWM) must be employed in the inversion stage. However, some drawbacks exist in this design as it brings additional switching losses in the inverter as well as a complex control circuitry.

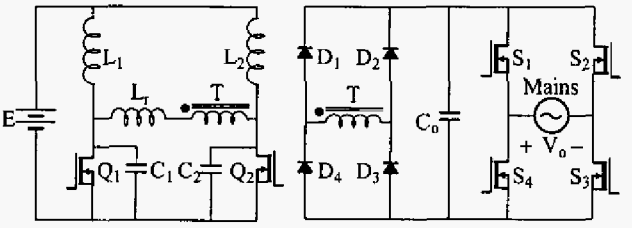

Fig. 1. The ZVS two-inductor boost converter with an inverter

This paper proposes a resonant two-inductor boost converter, where a two-phase synchronous buck converter acts as the current source for the ZVS boost cell, as shown in Fig. 2. The buck and the boost stages are interfaced through an interphase transformer (IPT). The resonant two-inductor boost cell operates under ZVS condition and produces an output with a rectified sinusoidal waveform. This reduces the following inversion stage to an unfolder with simple square-wave control.

This paper identifies the power loss terms that vary against the circuit parameters and numerically analyses the average power loss in the ZVS two-inductor boost cell operating under different circuit parameters. Then significant effort is made in the minimization of the total power loss in the ZVS boost cell. A resonant gate drive circuit is also employed in the converter to reduce the gate drive power in the boost stage under high switching frequency operations. The experimental results of a 1 MHz 100 W converter are provided at the end of the paper to prove the theoretical analysis.

II. THE CURRENT FED ZVS TWO-INDUCTOR BOOST CONVERTER

Although the voltage fed ZVS two-inductor boost converter is able to operate with a variable dc gain under variable frequency control, [4], a wide output range including zero voltage is not possible as it is a boost-derived converter. In order to achieve a variable output including zero voltage, a buck stage must be added. In the proposed converter shown in Fig. 2, a two-phase synchronous buck converter with an IPT functions as a variable current source to the ZVS boost cell so that a zero voltage can be achieved on the dc link. The employment of the IPT doubles the switching frequency of the buck conversion stage and avoids the penalty of the potential higher switching losses in the hard-switched buck converter.

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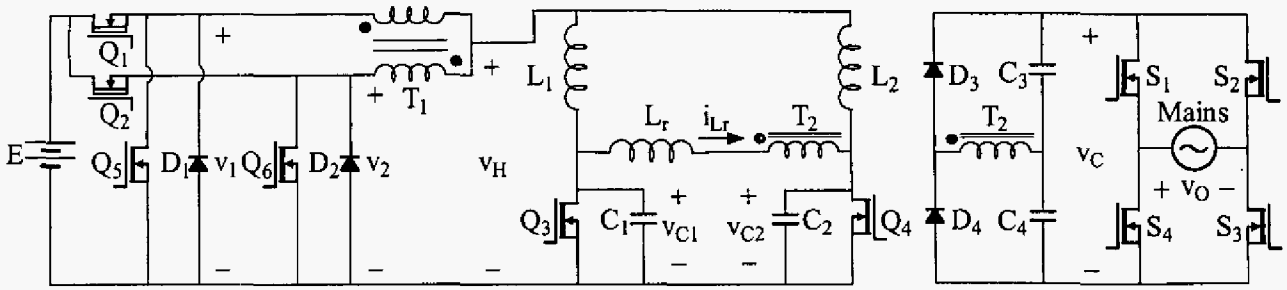


Fig. 2. The ZVS two-inductor boost converter with an unfolder

In the ZVS two-inductor boost cell, the transformer leakage inductance and the mosfet output capacitance are used as part of the resonant inductor L_r and capacitors C_1 and C_2. The resonance between the resonant inductor and capacitors creates a zero voltage switching condition for the mosfets and the switching loss can be completely removed, [3]. Three important circuit parameters, the load factor k, the timing factor Δ_1 and the delay angle α_d, determine the resonant condition of the ZVS boost cell [5] and are therefore the key parameters for the power loss analysis of the cell. A set of the resonant capacitor voltage and inductor current waveforms when $C_1 = C_2$ are shown in Fig. 3. The three circuit parameters are marked in the waveforms and explained below. The operation in Fig. 3 can be categorized as operation in Region 1, which is defined in the due course.

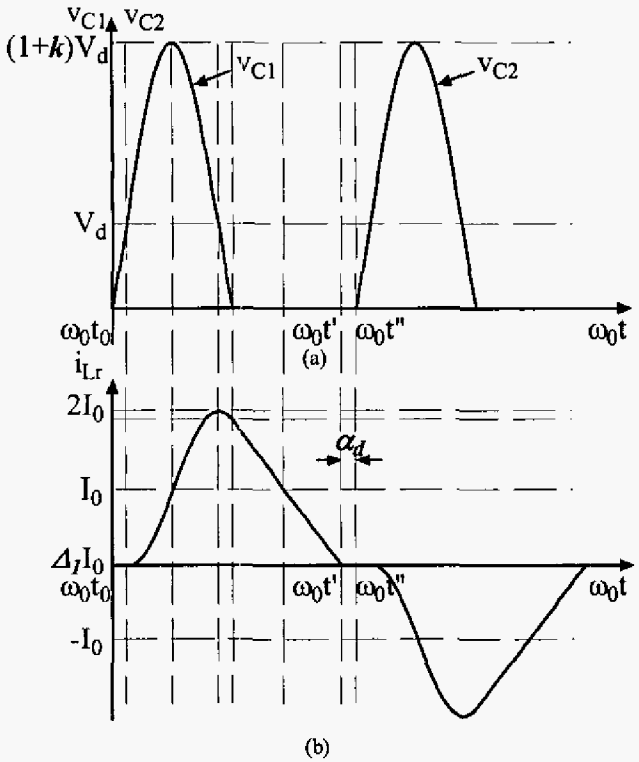


Fig. 3. The resonant waveforms in Region 1
(a) capacitor voltage (b) inductor current

- The load factor k, which is defined by $I_0 Z_0 = kV_d$, where I_0 is the input current in each inductor in the ZVS cell, Z_0 is the characteristic impedance of the resonant tank and V_d is the voltage across the capacitor C_3 or C_4 in the voltage doubler rectifier reflected to the transformer primary. It is required that k be greater than or equal to 1 to allow the resonant capacitor voltage to return to zero so that the ZVS condition can be maintained.

- The timing factor Δ_1, which determines the initial inductor current $i_{Lr}(\omega_0 t_0) = -\Delta_1 I_0$ when the mosfet Q_3 turns off. The initial inductor current is zero in the mode shown in Fig. 3.

- The delay angle α_d is the angle between the instant when the inductor current falls to zero and the instant when the corresponding mosfet turns off, which respectively corresponds to $\omega_0 t'$ and $\omega_0 t''$ in Fig. 3.

The ZVS cell is able to operate under two different regions: Region 1, where $\Delta_1 = 0$ and $\alpha_d \geq 0$ and Region 2, where $\Delta_1 \geq 0$ and $\alpha_d = 0$.

In order to maintain the resonant condition of the current fed ZVS two-inductor boost converter, some attention must be paid to the non-linearity of the mosfet output capacitance, [6]. The low frequency term of the input voltage to the ZVS boost cell V_H is a rectified sinusoidal waveform and this leads to different peak mosfet drain source voltages over a low frequency cycle under the same set of circuit parameters. One simple solution is to select a switching frequency which requires a relatively large additional resonant capacitance therefore the mosfet output capacitance only forms an insignificant portion of the total resonant capacitance. In this case, the variation of the mosfet output capacitance can be neglected.

III. The Resonant Mosfet Gate Drive Circuit

In the conventional mosfet gate drive circuit, the drive power loss is proportional to the switching frequency, [7]. Drive power is a significant portion of the total power loss when the switching frequency is high and this reduces the converter overall efficiency remarkably. The ZVS boost cell in the

proposed topology employs a resonant gate drive circuit with a theoretical zero drive power loss, as shown in Fig. 4, [8]. In the resonant gate drive circuit, two P type control mosfets Q_{3t} and Q_{4t} tie the gates of the power mosfets to the positive rail of the control power supply once the gate capacitances are charged to that level and two N type control mosfets Q_{3b} and Q_{4b} tie the gates of the power mosfets to the ground once the gate capacitances are fully discharged. A small inductor L_G between the mosfets Q_3 and Q_4 is added to transfer the energy between the two gate capacitances over the above charging and discharging periods.

In this resonant gate drive circuit, the mosfet input capacitances are charged by the inductor current during the turn-on and the turn-off transitions and no CV^2 loss occurs. Also a dead time is accomplished between the turn-ons of the control mosfets in the totem-pole to allow the build-up or the release of the charge on the power mosfet input capacitances. This easily prevents the cross conduction from happening. The switch timing of the control mosfets should be carefully designed so that they turn on or off at zero voltage or zero current, leading to zero switching loss for the control mosfets. Therefore, a theoretical zero power loss can be achieved. In the practical operation, however, a small amount of power loss does exist due to the component parasitic effects.

IV. The Power Loss Analysis of the ZVS Two-Inductor Boost Cell

In the physical construction of the ZVS two-inductor boost cell, the mosfets, the additional resonant inductor and the additional resonant capacitors are implemented by the components with the pre-determined electrical characteristics. Under different circuit parameters, different resonant voltage and current waveforms are established in the ZVS cell and the power loss term in each component varies. The transformer in the ZVS cell can be designed after the circuit parameters are selected and the transformer winding can be configured in a way to produce a fixed total copper and core loss. The power loss in the voltage doubler rectifier of the ZVS cell is only load sensitive and will not vary against different circuit parameters. Therefore in order to achieve a minimum total power loss in the ZVS two-inductor boost cell, only the variable power loss components of the mosfets, the resonant inductor and the resonant capacitors need to be considered and they can be expressed by (1) to (3).

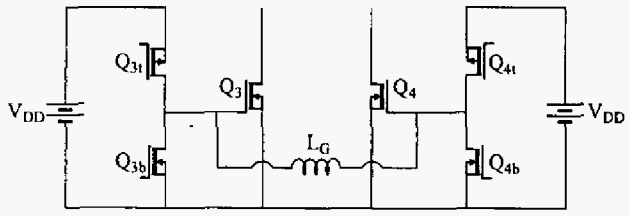


Fig. 4. The resonant gate drive for the two-inductor boost cell

- The power loss in the two mosfets p_Q:

$$p_Q = 2(I_{Q,rms}^2 \cdot R_{DS(on)} + I_{Q,avg} \cdot V_F) \quad (1)$$

where $I_{Q,rms}$ is the effective forward current in the mosfet, $R_{DS(on)}$ is the mosfet forward resistance, $I_{Q,avg}$ is the average reverse current in the mosfet and V_F is the forward voltage drop of the mosfet body diode.

- The power loss in the resonant inductor p_{Lr}:

$$p_{Lr} = I_{Lr,rms}^2 \cdot R_{Lr} \quad (2)$$

where $I_{Lr,rms}$ is the effective current in the resonant inductor and R_{Lr} is the series dc plus ac resistance of the resonant inductor.

- The power loss in the two resonant capacitors p_{Cr}:

$$p_{Cr} = 2I_{Cr,rms}^2 \cdot R_{Cr} \quad (3)$$

where $I_{Cr,rms}$ is the effective current in the resonant capacitor and R_{Cr} is the Equivalent Series Resistance (ESR) of the resonant capacitors.

The total power loss p_t over a high frequency switching cycle which alters with different circuit parameters in the ZVS boost cell is:

$$p_t = p_Q + p_{Lr} + p_{Cr} \quad (4)$$

As the input voltage of the ZVS cell is modulated in the sinusoidal manner, the average power loss over a low frequency sinusoidal cycle, P_{avg}, must be established in order to identify the operating point with the minimum power loss in the ZVS cell. The process can be performed numerically with the MATLAB program.

In order to calculate the variable power loss components in the ZVS cell, a variety of the current terms and the equivalent series resistances of the resonant inductor and capacitors in (1) to (3) must be obtained. The current terms can be obtained through the state analysis of the equivalent resonant circuit while the series resistance of the resonant inductor and the ESR of the resonant capacitors are not directly obtained. The resistance terms must be further derived with two other direct results through the state analysis.

- The quotient of the resonant tank angular frequency, ω_0, and the switching frequency of the boost cell, f_{boost}:

$$\gamma = \frac{\omega_0}{f_{boost}} \tag{5}$$

- The resonant tank characteristic impedance:

$$Z_0 = \frac{k \cdot V_d}{I_0} \tag{6}$$

The definitions of the series dc plus ac resistance of the resonant inductor, the ESR of the resonant capacitor and the resonant tank characteristic impedance are respectively given in (7) to (9).

$$R_{Lr} = \frac{2\pi f_{boost} L_r}{Q} \tag{7}$$

$$R_{Cr} = \frac{DF}{2\pi f_{boost} C_r} \tag{8}$$

$$Z_0 = \sqrt{\frac{L_r}{C_r}} = \omega_0 L_r = \frac{1}{\omega_0 C_r} \tag{9}$$

where L_r is the resonant inductance, $C_1 = C_2 = C_r$ is the resonant capacitance, Q is the quality factor of the resonant inductor and DF is the dissipation factor of the resonant capacitor.

Manipulations of (5) to (9) yield

$$R_{Lr} = \frac{2\pi \cdot Z_0}{Q \cdot \gamma} \tag{10}$$

$$R_{Cr} = \frac{DF \cdot \gamma \cdot Z_0}{2\pi} \tag{11}$$

In the numerical calculation of the average power loss in the ZVS boost cell, the following component parameters are used.

- $R_{DS(on)} = 0.027\ \Omega$ and $V_F = 1.5\ V$ for STB50NE10 mosfets,
- $Q = 96$ at 500 kHz for the air core toroidal inductor with Litz wire,
- $DF = 1/6000$ at 500 kHz for Cornell Dubilier surface mount mica capacitors.

It is worth mentioning that as the transformer leakage inductance and the mosfet output capacitance respectively forms part of the resonant inductor and capacitors, the actual power losses of these components will be different from the results obtained through (2) and (3) if the above component parameters are used. However, under the assumption that the values of the parasitic components are relatively small compared with the resonant inductance and capacitance values, the errors in the results of (2) and (3) are unlikely to be large.

Figs. 5 and 6 respectively shows the surface of the average power loss $P_{avg,\Delta}$ in Region 2 and $P_{avg,\alpha}$ in Region 1 in the ZVS cell with an average power of 100 W at a 500 kHz device switching frequency. Fig. 5 shows the average power loss when $1 \le k \le 4$ and $0 \le \Delta_1 \le 2$. In this region, the lowest average power loss occurs when $k = 1$ and $\Delta_1 = 0$, which is 2.21 W.

Fig. 6 shows the average power loss when $1 \le k \le 4$ and $0 \le \alpha_d \le 4$. In this region, the average power loss can be further lowered. It can be observed that under the same k value, the greater the α_d value, the lower the average power loss. However, a higher peak switch voltage appears while α_d increases as shown by the surface $V_{peak,\alpha}$ in Fig. 7. A peak switch voltage of 100 V is set in the converter operation to obtain a low mosfet forward resistance. Mosfet input capacitance increases considerably for the same value of the forward resistance at a higher voltage rating as the product of the input capacitance and forward resistance increases with drain-source voltage rating, [9]. A larger mosfet input capacitance either demands a higher power from the conventional drive circuit or results in additional loss related to the parasitic components in the resonant drive circuit proposed in [8] and this lowers the converter overall efficiency. Another reason to choose a lower α_d value is that the gradient of the surface $P_{avg,\alpha}$ along the α_d axis is very small. When $k = 1$ and $0 \le \alpha_d \le 4$, the average gradient of the power loss against α_d is -0.11 W/radian, while that of the peak switch voltage against α_d is 12.9 V/radian. Figs. 6 and 7 show that the changes of the power loss and the peak switch voltage along the α_d axis under the same k value are both monotonic. The ZVS operating condition requires $k \ge 1$. The final circuit parameters for the minimal power loss in the ZVS boost cell are $k = 1.1$, $\Delta_1 = 0$ and $\alpha_d = 0$. Under this condition, the average power loss is 2.33 W and the peak switch voltage is 90 V. The safety margin for k to maintain the ZVS condition is justified by the numerical results from MATLAB, which show that the increase of k from 1 to 1.1 when $\Delta_1 = 0$ and $\alpha_d = 0$ only raises the average power loss by an insignificant amount of 0.12 W. Once the circuit parameters are determined, other important values in designing the ZVS cell can be obtained as the following:

- The resonant inductance $L_r = 1.40\ \mu H$,
- The resonant capacitance $C_r = 15.7\ nF$,
- The gain of the transformer primary to the ZVS boost cell input voltages $V_d / v_H = 2.15$.

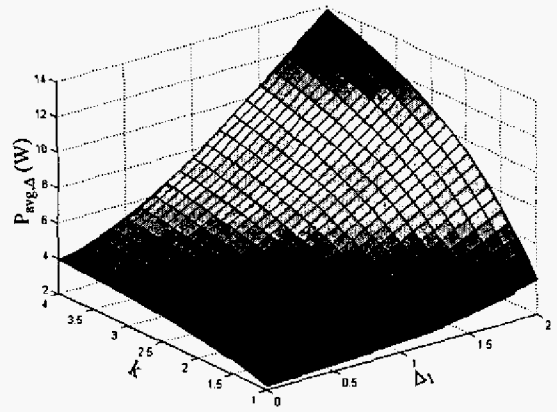


Fig. 5. Surface $P_{avg,\Delta}$

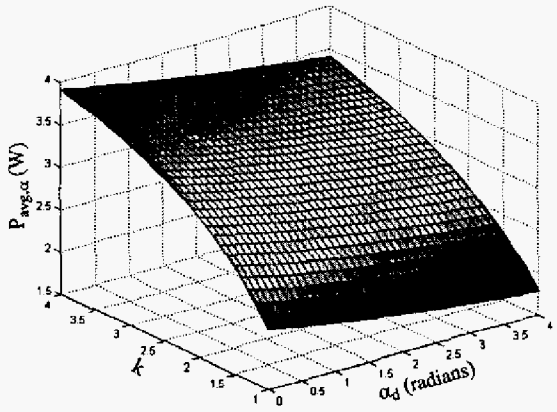


Fig. 6. Surface $P_{avg,\alpha}$

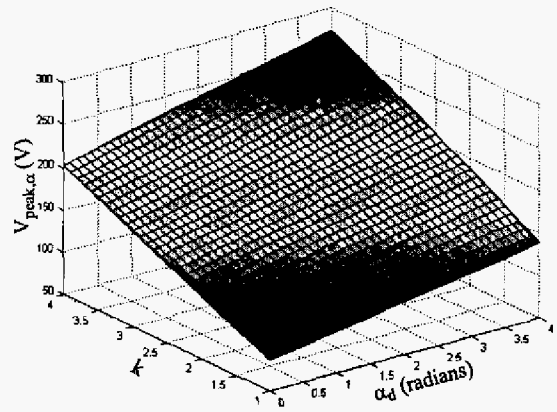


Fig. 7. Surface $V_{peak,\alpha}$

V. Experimental Waveforms

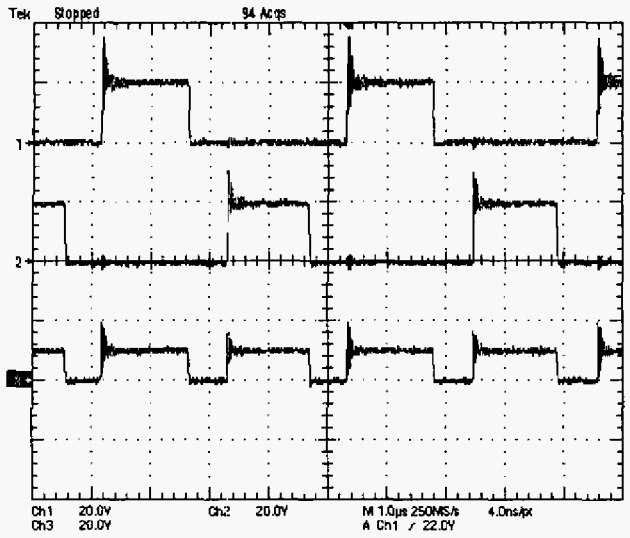
In order to prove the theoretical analysis, a prototype converter is built in the laboratory. The device switching frequency of the buck stage mosfets f_{buck} is 250 kHz, resulting in a current ripple frequency of 500 kHz after the IPT. In the converter, a Linear Technology two-phase synchronous step-down switching regulator LTC1929CG is used to simplify the design of the synchronous buck converter. The gate signals in the buck converter are synchronized through a frequency divider from the gate signals in the two-inductor boost cell. The IPT is implemented by an Epcos EFD15 core with 14 turns on both primary and secondary sides.

The boost stage operates with a converter frequency of 1 MHz, which corresponds to a mosfet device switching frequency f_{boost} of 500 kHz. In the ZVS boost cell, the two inductors are wound onto a single Ferroxube ETD29 core with 0.5 mm air gaps on both outer legs to achieve space saving. The SiC diodes are used in the voltage doubler rectifier to avoid the power loss associated with the reverse recovery. In the unfolder, the photovoltaic mosfet drivers are used to drive the mosfets in the full bridge inverter. Figs. 8 to 12 show the experimental waveforms.

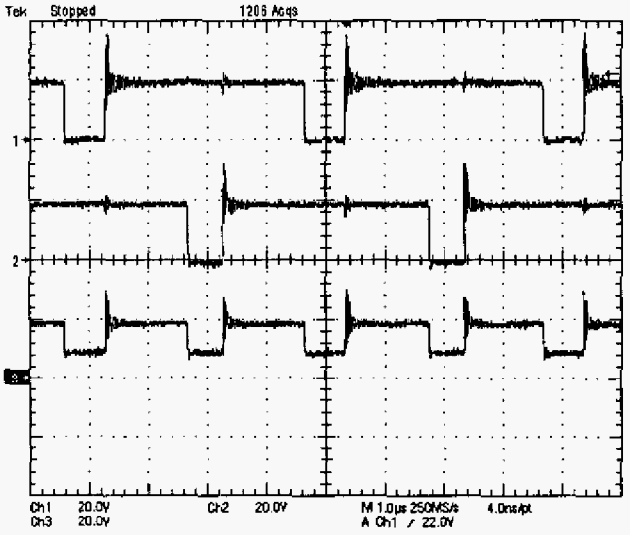
Fig. 8 shows the buck converter waveforms under static tests. From top to bottom, Figs. 8(a) and (b) respectively shows the waveforms of v_1, v_2 and v_H with the duty ratio smaller or greater than 50%. The voltage after the IPT swings between zero and half input voltage when the duty ratio of the buck stage mosfets $D_{buck} < 50\%$ and swings between half and full input voltages when $D_{buck} > 50\%$. In both cases, the frequency of the voltage after the IPT is twice those of the two voltages before.

Fig. 9 shows the two-inductor boost converter output voltage v_C and the input voltage v_H from top to bottom during the sinusoidal modulation. A three-level modulation can be obviously observed in the v_H waveform although the waveform captured by the oscilloscope is heavily aliased.

Fig. 10 shows the gate waveforms of the low frequency unfolder switches and the output voltage v_O from top to bottom. In this case a resistive load is supplied and this is adjusted to give the rated power, 100 W average, at 240 V ac, which is equivalent to the nominal mains voltage. A conversion efficiency of 91% was obtained for the module integrated PV converter power train. The power loss includes the losses in the buck stage, the ZVS cell and the unfolder stage. Input and output powers were measured using the mathematical functions of a Tektronix TDS5034 four-channel oscilloscope equipped with converter input and output voltage and current probes. The current probes are Tektronix TCP202.



(a)



(b)

Fig. 8. Two-phase synchronous buck converter waveforms
(a) $D_{buck} < 50\%$ (b) $D_{buck} > 50\%$

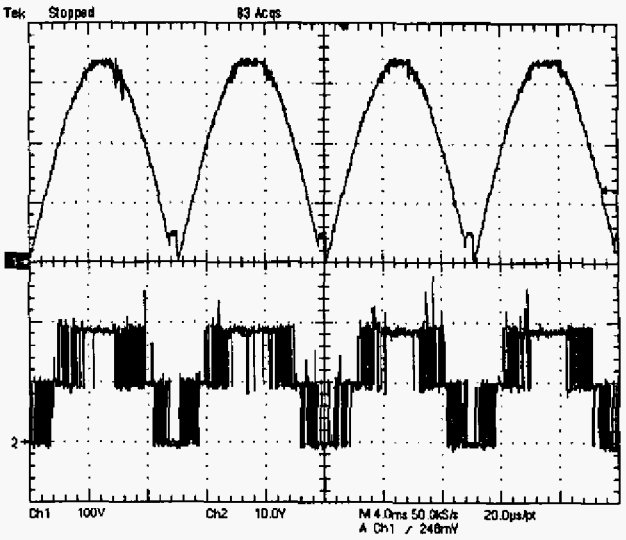


Fig. 9. Sinusoidal modulation waveforms

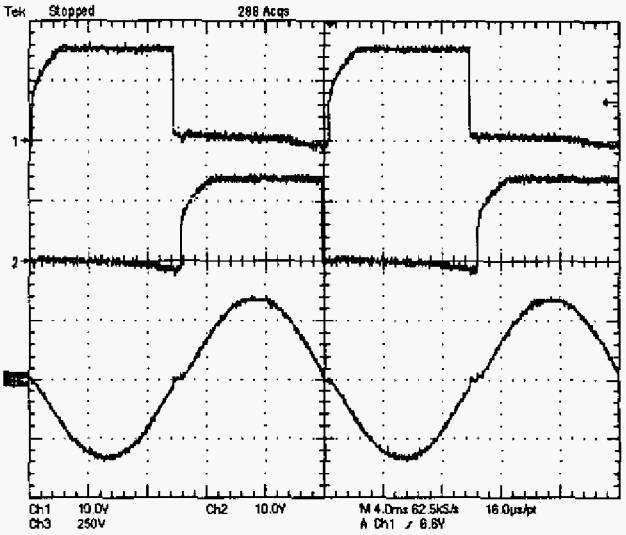


Fig. 10. Low frequency unfolder waveforms

From top to bottom, Fig. 11 shows the gate and drain voltage waveforms of the mosfets in the ZVS two-inductor boost cell when the output voltage is close to the peak. The mosfet drain source voltage waveforms confirm that the mosfets turn on at zero voltage.

Fig. 12 shows the voltage across the diode in the voltage doubler when the output voltage is close to the peak. The waveform is relatively clean. No reverse recovery can be seen in the silicon carbide Schottky rectifiers although some lower frequency oscillations with an approximately 200 ns period can be seen. These are driven by the charging of the diode junction capacitance via the transformer leakage inductance.

VI. Conclusions

In this paper, a current fed ZVS two-inductor boost converter with an unfolder is proposed as a voltage boosting and galvanic isolation stage for a module integrated PV converter. The ZVS boost cell is fed with a rectified sinusoid modulated current by a two-phase synchronous buck converter. The ZVS cell operates under a loss optimised set of conditions at fixed frequency and produces a rectified sinusoidal output waveform. This is converted to a mains compatible sinusoidal current by a low frequency unfolding stage.

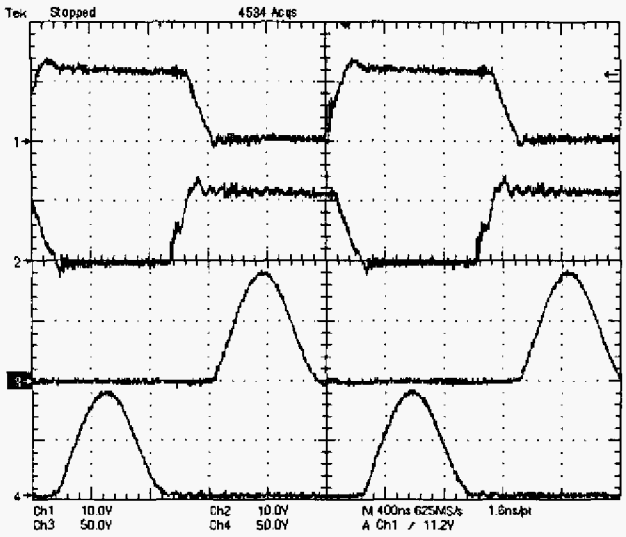


Fig. 11. Mosfets gate and drain voltages

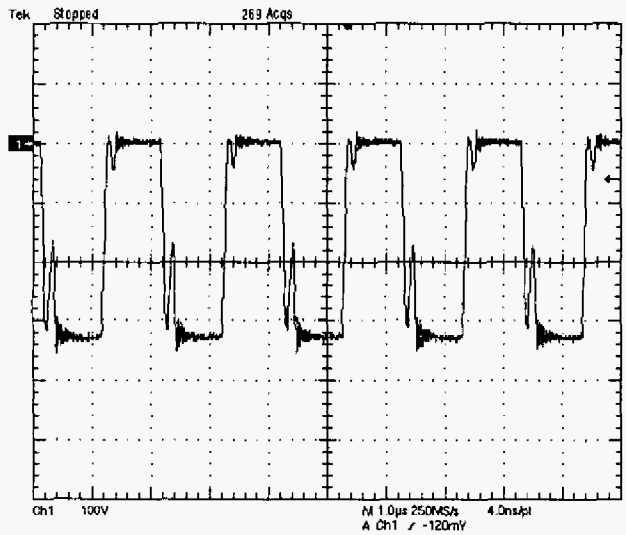


Fig. 12. Diode voltage

In order to achieve the minimal power loss in the ZVS boost cell, this paper proposes a power loss optimisation method. A set of power loss terms that vary with different circuit parameters in the ZVS cell is identified and a numerical analysis of the average power loss is conducted. Finally, the optimised operating point with the lowest power loss is determined with the aid of the visual surfaces showing the average power losses in the two operating regions.

The theoretical analysis is validated by a prototype ZVS converter with a 1 MHz converter switching frequency and an average power of 100 W. The ZVS two-inductor boost cell also employs a resonant gate drive, which reduces the drive power remarkably under high switching frequency operations.

The cell is integrated within a module integrated PV converter, which achieves an overall efficiency of 91% for a power train that includes the two-phase buck converter stage, the ZVS cell and the output unfolder stage.

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